DK_START_GW5AT-LV60PG484A_V1.1

User Guide

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Revision History

Date	Version	Description
12/31/2024	1.0E	Initial version published.
05/09/2025	1.0.1E	The “Figure 2-3 PCB Components” updated.

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1 About This Guide

1.1 Purpose

The DK_START_GW5AT-LV60PG484A_V1.1 development board (hereinafter referred to as “the development board”) user guide consists of following three parts:

- A brief introduction to the features of the development board
- An introduction to the development board system architecture and hardware resources
- An introduction to the hardware circuits, functions and pin distribution

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS981, GW5AT series of FPGA Products Data Sheet
- UG1222, GW5AT-60 Pinout
- UG983, GW5AT series of FPGA Products Package and Pinout User Guide
- UG718, Arora V 60K FPGA Products Programming and Configuration User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
ADC	Analog-to-digital Converter
SFP	Small Form-factor Pluggable Transceivers
DDR	Double Data Rate
JTAG	Joint Test Action Group
SDI	Serial Digital Interface
LDO	Low Dropout Regulator

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

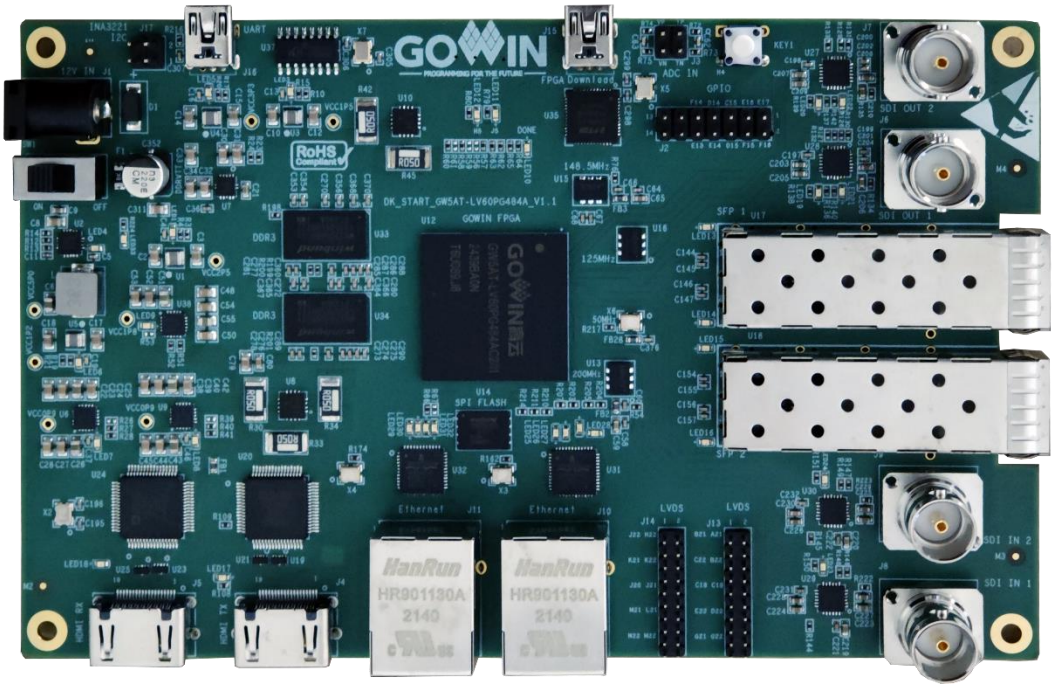
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_START_GW5AT-LV60PG484A_V1.1 Development Board



Gowin GW5AT series of FPGA products are the 5 series products of Arora family, with abundant internal resources, high-performance DSP with a new architecture that supports AI operations, high-speed LVDS interface and abundant BSRAM resources. At the same time, it integrates self-developed DDR3, and provides a variety of packages. It is suitable for applications such as low power, high performance and compatibility design.

DK_START_GW5AT-LV60PG484A_V1.1 development board applies to DDR3 high-speed storage, MIPI and SFP high-speed communication,

integrates LVDS, SDI-IN, SDI-OUT, Ethernet, HDMI-TX, HDMI-RX, and ADC interfaces, supporting FPGA function evaluation, hardware verification, and software learning and debugging, etc.

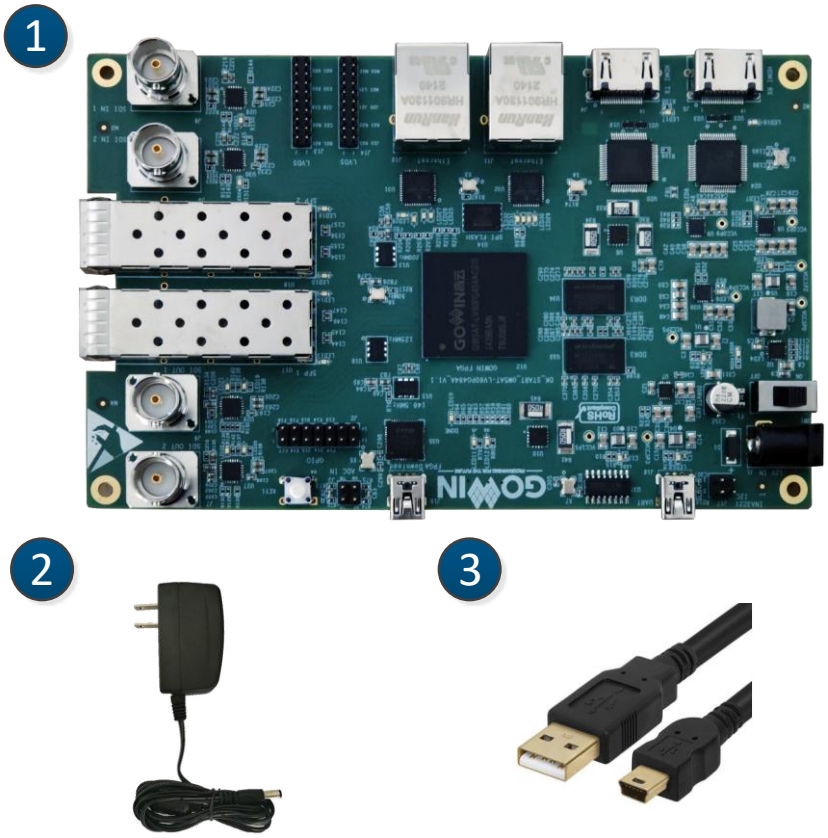
The development board adopts Gowin GW5AT-LV60PG484A FPGA device. For the internal resources of the chip, see *DS981, GW5AT series of FPGA Products Data Sheet*.

2.2 A Development Board Kit

The development board kit includes the following items:

1. DK_START_GW5AT-LV60PG484A_V1.1 development board
2. 12V power (Input: AC 100-240V~50/60Hz 0.6A, output: DC12V 2A)
3. Mini USB-B download cable

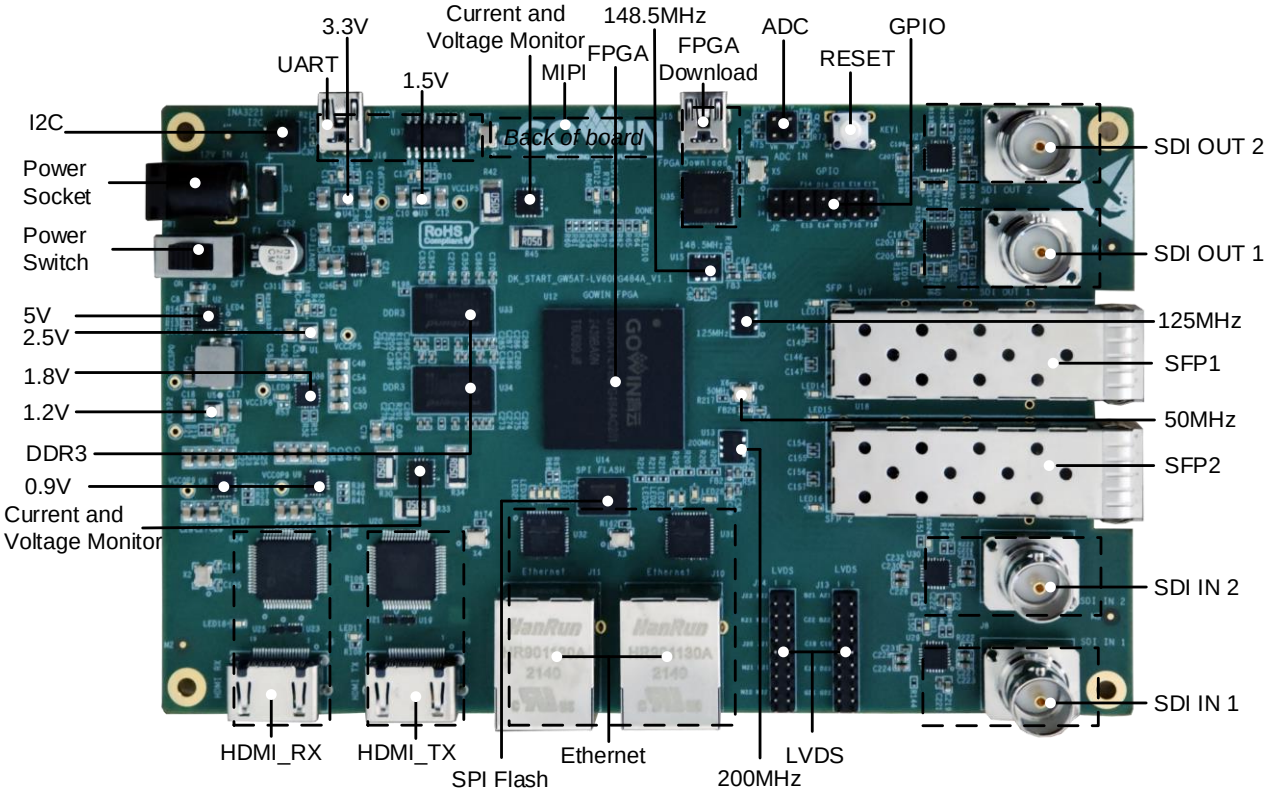
Figure 2-2 A Development Board Kit



① DK_START_GW5AT-LV60PG484A_V1.1 development board
② 12V power supply adapter
③ Mini USB-B Cable

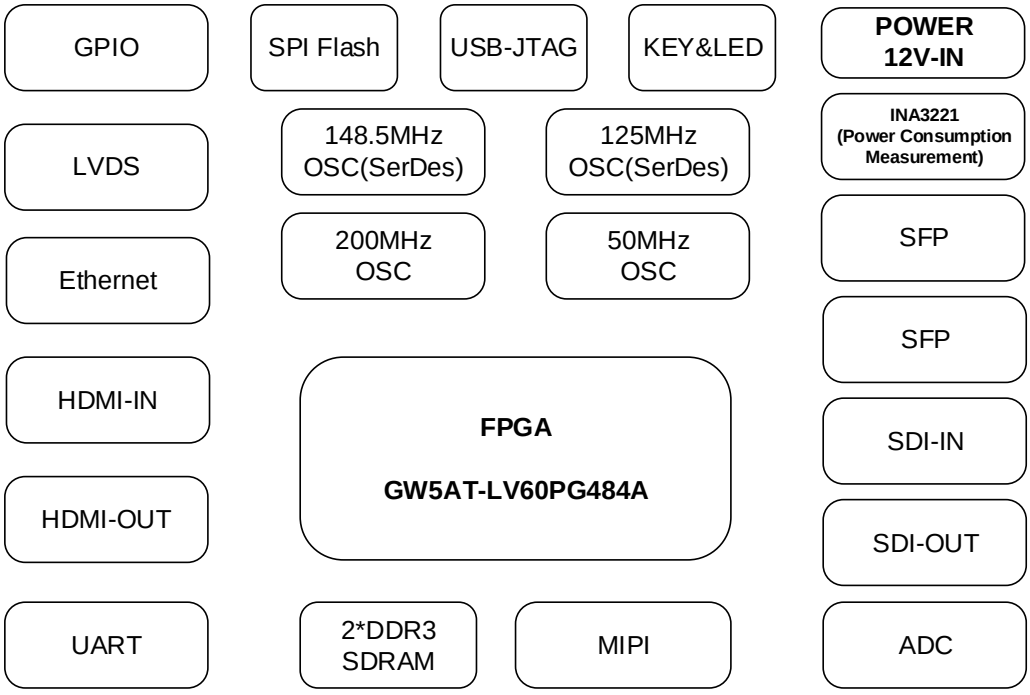
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Block Diagram

Figure 2-4 System Block Diagram



2.5 Features

The key features are as follows:

- FPGA Device
  - Gowin GW5AT-LV60PG484A FPGA
- Download and Boot
  - Integrate USB download circuit on the development board, download through Mini USB-B interface
  - External SPI Flash Boot
- Power
  - External DC 12V 2A Power
  - The Power light is on after power on.
  - The board generates 5V, 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, 0.9V, 0.75V power.
- Clock system
  - 50MHz single-ended clock
  - 125MHz differential clock
  - 148.5MHz differential clock
  - 200MHz differential clock
- Memory device
  - 4Gbit DDR3 SDRAM
  - 256Mbit NOR Flash
- SFP Interface
  - 2-channel SFP connectors for SFP or SFP+ modules
- HDMI Interface
  - 1-channel HDMI-TX interface for HDMI-TX communication via the encoding chip
  - 1-channel HDMI-RX interface for HDMI-RX communication via the decoding chip
- SDI Interface
  - Two SDI-IN interfaces
  - Two SDI-OUT interfaces
  - 6G SDI interface supporting 5.94 Gbps SDI data transfer
- Ethernet Interface
  - Two Ethernet interfaces
  - Support RGMII interfaces (10Base-T/100Base-T/1000BASE-T)
  - RJ45 connector integrated with network transformer internally
- MIPI Interface
  - MIPI interface with dual channels, each channel includes 4 data + 1 clk

  - 4 GPIOs with 3.3V voltage level standard reserved
- LVDS Interface
  - 2-channel LVDS interfaces, each channel including 4 data + 1 clk
- I2C Interface
  - 1-channel I2C interface
- UART Interface
  - 1-channel UART interface
  - Mini USB-B connector
- ADC Interface
  - 1-channel ADC interface
- Key & Indicator
  - 1 low-level reset key
  - 2 LED indicators
- GPIO
  - 10 GPIOs with 3.3V voltage level standard

3 Development Board Circuit

3.1 FPGA

Overview

For the resources of GW5AT series of FPGA Products, refer to *DS981, GW5AT series of FPGA Products Data Sheet*.

I/O BANK Description

For the I/O BANK, package, and pinout information, see *UG983, GW5AT series of FPGA Products Package and Pinout User Guide* for more details.

3.2 Power Supply

3.2.1 Introduction

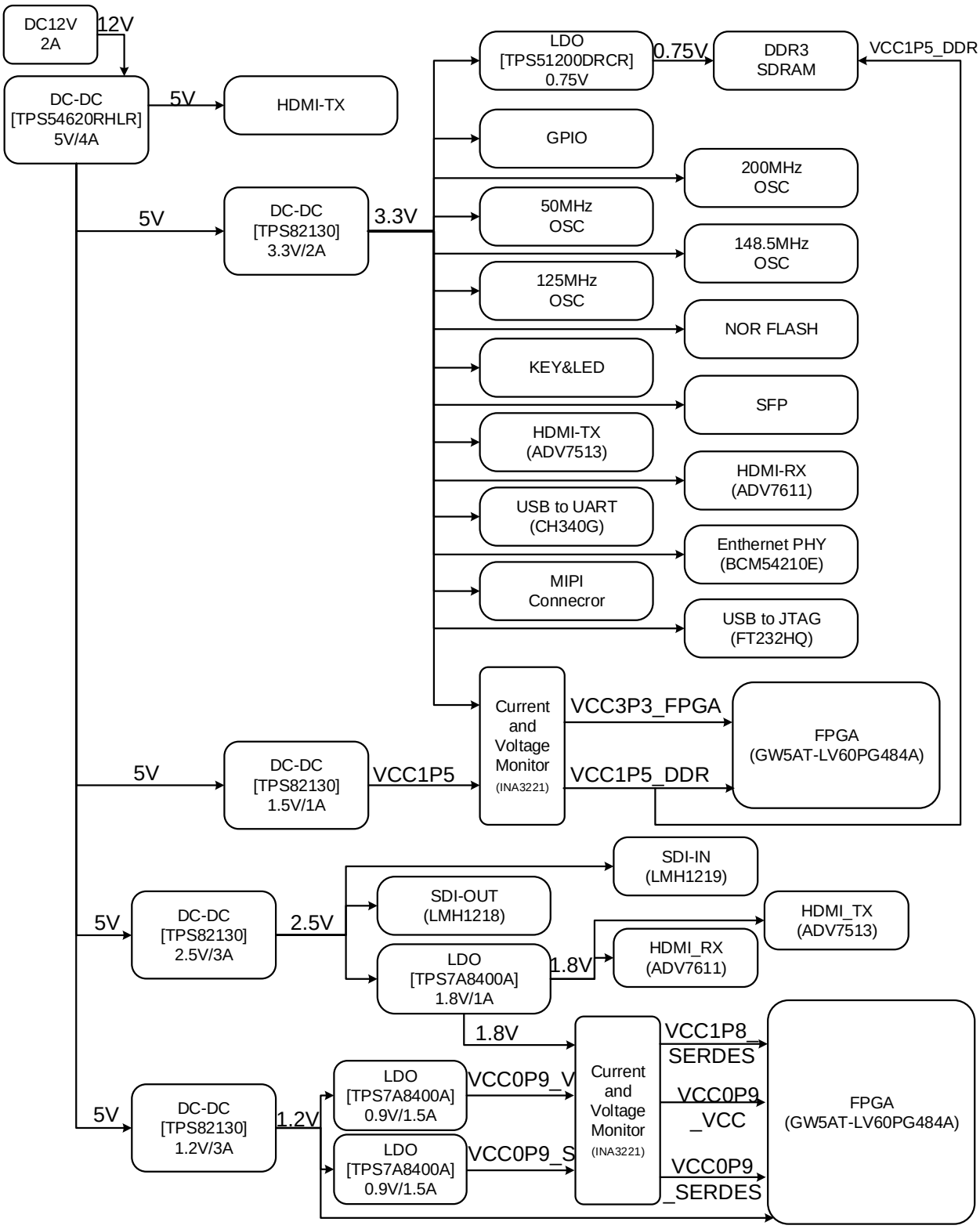
The development board needs to be powered by a 12V power adapter.

The input parameter of the adapter is AC 100-240V~50/60MHz 0.6A, and the output parameter is DC 12V 2A.

The input 12V power is regulated by the PMIC on the development board to generate 5V, 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, 0.9V, and 0.75V power supplies, thus meeting the power supply requirements of the development board.

3.2.2 Power Distribution

Figure 3-1 Power Distribution Diagram



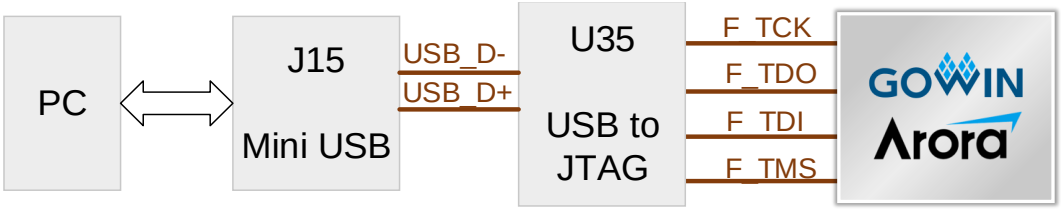
3.3 Download Module

3.3.1 Introduction

The development board includes a Mini USB-B download port (J15) designed to program the programs to external SPI FLASH or SRAM.

The download connection diagram is show in Figure 3-2.

Figure 3-2 Connection Diagram of Download



3.3.2 Pin Distribution

Table 3-1 JTAG Pin Distribution

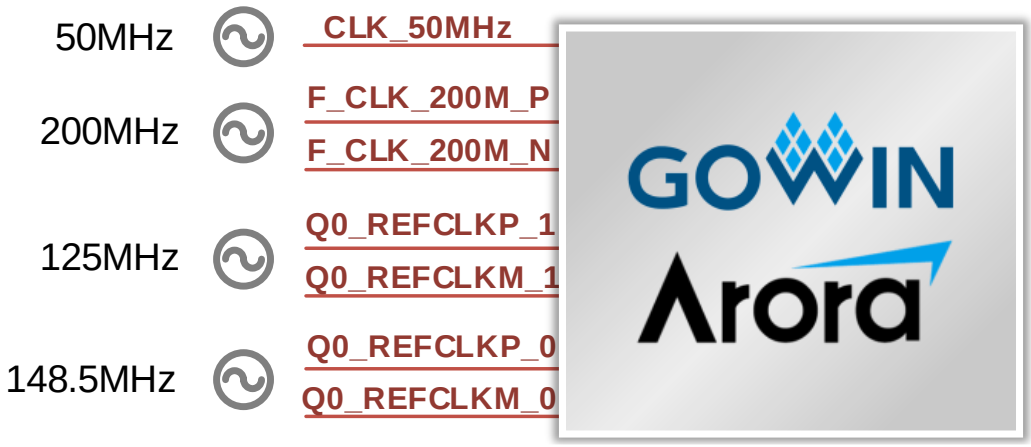
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_TCK	V12	12	3.3V	JTAG signal
F_TDO	U13	12	3.3V	
F_TDI	R13	12	3.3V	
F_TMS	T13	12	3.3V	

3.4 Clock

3.4.1 Introduction

The development board includes multiple FPGA clock sources, including 1-channel 50 MHz single-ended clock, 1-channel 200 MHz differential clock, 1-channel 125 MHz differential clock, and 1-channel 148.5 MHz differential clock. Among them, the 125 MHz and the 148.5 MHz differential clocks are connected the FPGA SerDes high-speed clock pins. The clock pin distribution is shown in Figure 3-3.

Figure 3-3 Clock Connection Diagram



3.4.2 Pin Distribution

Table 3-2 Clock Pin Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
CLK_50MHz	F13	1	3.3V	50MHz single-ended clock
F_CLK_200M_P	D17	1	3.3V	200MHz differential clock
F_CLK_200M_N	C17	1	3.3V	200MHz differential clock
Q0_REFCLKP_1	F10	Q0	-	125MHz differential clock
Q0_REFCLKM_1	E10	Q0	-	125MHz differential clock
Q0_REFCLKP_0	F6	Q0	-	148.5MHz differential clock
Q0_REFCLKM_0	E6	Q0	-	148.5MHz differential clock

3.5 DDR3

3.5.1 Introduction

The development board includes two 2 Gbit DDR3 chips. The signal of DDR3 chip is connected to the BANK9 and BANK10 of FPGA. The specific configurations of DDR3 are as shown in Table 3-3.

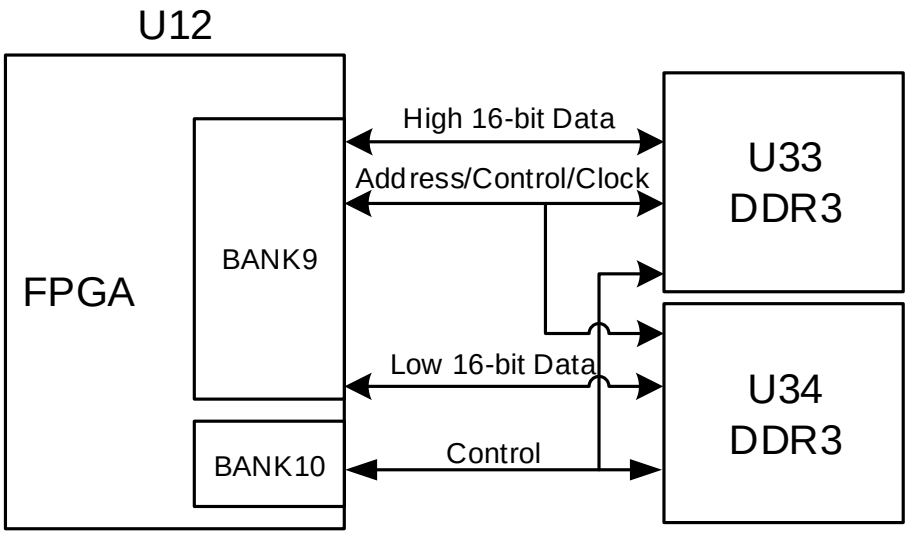
Table 3-3 DDR3 Configuration

Designator	Capacity
U33	128M x 16bit
U34	128M x 16bit

DDR3 hardware design requires strict consideration of signal integrity. In the design of circuit and PCB, matching resistor/termination resistor, impedance control and equal length control of traces have been fully considered to ensure DDR3 works stably at high speed.

The hardware connection diagram of DDR3 is as show in Figure 3-4.

Figure 3-4 Hardware Connection Diagram of DDR3



3.5.2 Pin Distribution

Table 3-4 DDR3 Pin Distribution

Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
DDR3_A0	AA10	9	1.5V	Address
DDR3_A1	Y12	9	1.5V	Address
DDR3_A2	W10	9	1.5V	Address
DDR3_A3	Y2	9	1.5V	Address
DDR3_A4	AA13	9	1.5V	Address
DDR3_A5	AB10	9	1.5V	Address
DDR3_A6	Y13	9	1.5V	Address
DDR3_A7	AB11	9	1.5V	Address
DDR3_A8	Y14	9	1.5V	Address
DDR3_A9	AA11	9	1.5V	Address
DDR3_A10	AB12	9	1.5V	Address
DDR3_A11	W11	9	1.5V	Address
DDR3_A12	W12	9	1.5V	Address
DDR3_A13	Y11	9	1.5V	Address
DDR3_BA0	V4	9	1.5V	Bank address
DDR3_BA1	AB13	9	1.5V	Bank address
DDR3_BA2	U2	9	1.5V	Bank address
DDR3_CS#	P1	10	1.8V	Chip select
DDR3_CAS#	U7	9	1.5V	Column address strobe
DDR3_CKE	R1	10	1.8V	Clock enable
DDR3_ODT	N2	10	1.8V	On-Die Termination Enable
DDR3_RAS#	AA9	9	1.5V	Row address strobe
DDR3_RESET	P2	10	1.8V	Reset
DDR3_WE#	R4	9	1.5V	Write enable

Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
DDR3_CLK_P	V7	9	1.5V	Differential clock
DDR3_CLK_N	W7	9	1.5V	Differential clock
DDR3_DQ0	AB7	9	1.5V	Data
DDR3_DQ1	Y8	9	1.5V	Data
DDR3_DQ2	Y7	9	1.5V	Data
DDR3_DQ3	W9	9	1.5V	Data
DDR3_DQ4	AB8	9	1.5V	Data
DDR3_DQ5	V10	9	1.5V	Data
DDR3_DQ6	AB6	9	1.5V	Data
DDR3_DQ7	AA8	9	1.5V	Data
DDR3_DQ8	T5	9	1.5V	Data
DDR3_DQ9	Y6	9	1.5V	Data
DDR3_DQ10	U6	9	1.5V	Data
DDR3_DQ11	T4	9	1.5V	Data
DDR3_DQ12	T6	9	1.5V	Data
DDR3_DQ13	AA6	9	1.5V	Data
DDR3_DQ14	R6	9	1.5V	Data
DDR3_DQ15	U5	9	1.5V	Data
DDR3_DQ16	AB1	9	1.5V	Data
DDR3_DQ17	AA4	9	1.5V	Data
DDR3_DQ18	AA1	9	1.5V	Data
DDR3_DQ19	AA5	9	1.5V	Data
DDR3_DQ20	AB2	9	1.5V	Data
DDR3_DQ21	W4	9	1.5V	Data
DDR3_DQ22	AB3	9	1.5V	Data
DDR3_DQ23	Y4	9	1.5V	Data
DDR3_DQ24	W2	9	1.5V	Data
DDR3_DQ25	V2	9	1.5V	Data
DDR3_DQ26	U3	9	1.5V	Data
DDR3_DQ27	U1	9	1.5V	Data

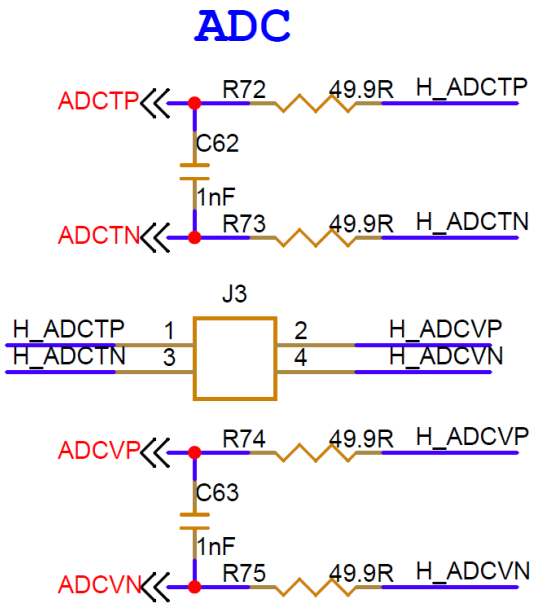
Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
DDR3_DQ28	Y1	9	1.5V	Data
DDR3_DQ29	T3	9	1.5V	Data
DDR3_DQ30	V3	9	1.5V	Data
DDR3_DQ31	T1	9	1.5V	Data
DDR3_LDM0	Y9	9	1.5V	Data input mask
DDR3_UDM0	V5	9	1.5V	Data input mask
DDR3_LDQS0_P	V9	9	1.5V	Data clock
DDR3_LDQS0_N	V8	9	1.5V	Data clock
DDR3_UDQS0_P	W6	9	1.5V	Data clock
DDR3_UDQS0_N	W5	9	1.5V	Data clock
DDR3_LDM1	AB5	9	1.5V	Data input mask
DDR3_UDM1	W1	9	1.5V	Data input mask
DDR3_LDQS1_P	Y3	9	1.5V	Data clock
DDR3_LDQS1_N	AA3	9	1.5V	Data clock
DDR3_UDQS1_P	R3	9	1.5V	Data clock
DDR3_UDQS1_N	R2	9	1.5V	Data clock

3.6 ADC Interface

3.6.1 Introduction

The development board includes input interfaces for ADC signals. The connector uses a 2x2P pin header with 2.54 mm pitch. Figure 3-5 is the ADC interface schematic connection diagram and the anti-aliasing filter circuit.

Figure 3-5 Connection Diagram of ADC Interface Schematic



3.6.2 Pin Distribution

Table 3-5 Pin Distribution of ADC Interface

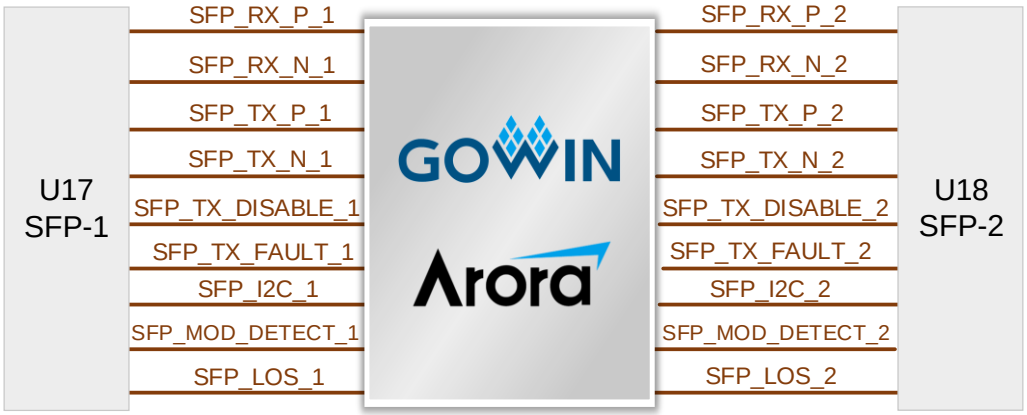
J3 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	ADCTP	N10	ADC	-	Analog signal input
2	ADCVP	L10	ADC	-	Analog signal input
3	ADCTN	N9	ADC	-	Analog signal input
4	ADCVN	M9	ADC	-	Analog signal input

3.7 SFP Interface

3.7.1 Introduction

The development board includes two SFP interfaces for SFP or SFP+ modules. The design diagram is shown in Figure 3-6.

Figure 3-6 Connection Diagram of SFP Interface



3.7.2 Pin Distribution

Table 3-6 Pin Distribution of SFP-1 Interface

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
SFP_RX_P_1	D9	Q0	-	Receive partial differential signal outputs
SFP_RX_N_1	C9	Q0	-	Receive partial differential signal outputs
SFP_TX_P_1	D7	Q0	-	Transmit partial differential signal inputs
SFP_TX_N_1	C7	Q0	-	Transmit partial differential signal inputs
SFP_TX_FAULT_1	E2	11	3.3V	Transmitting error
SFP_TX_DISABLE_1	G2	11	3.3V	Shutdown enable input
SFP_IIC_SDA_1	D1	11	3.3V	I2C data bus
SFP_IIC_SCL_1	E1	11	3.3V	I2C clock bus
SFP_MOD_DETECT_1	F1	11	3.3V	Module presence

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
				detection
SFP_RS0_1	-	-	-	Rate selection
SFP_RS1_1	-	-	-	Rate selection
SFP_LOS_1	G1	11	3.3V	Receiver losts the indicator signals.

Table 3-7 Pin Distribution of SFP-2 Interface

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
SFP_RX_P_2	D11	Q0	-	Receive partial differential signal outputs
SFP_RX_N_2	C11	Q0	-	Receive partial differential signal outputs
SFP_TX_P_2	D5	Q0	-	Transmit partial differential signal inputs
SFP_TX_N_2	C5	Q0	-	Transmit partial differential signal inputs
SFP_TX_FAULT_2	F4	11	3.3V	Transmitting error
SFP_TX_DISABLE_2	G4	11	3.3V	Shutdown enable input
SFP_IIC_SDA_2	E3	11	3.3V	I2C data bus
SFP_IIC_SCL_2	F3	11	3.3V	I2C clock bus
SFP_MOD_DETECT_2	G3	11	3.3V	Module presence detection
SFP_RS0_2	-	-	-	Rate selection
SFP_RS1_2	-	-	-	Rate selection
SFP_LOS_2	D2	11	3.3V	Receiver losts the indicator signals.

3.8 HDMI Interface

3.8.1 Introduction

The development board leads 1-channel HDMI-TX interface and 1-channel HDMI-RX interface. The HDMI input and output communication is implemented via the decoding and encoding chips, respectively. The connection diagram of HDMI interface is as follows.

Figure 3-7 Connection Diagram of HDMI_TX Interface

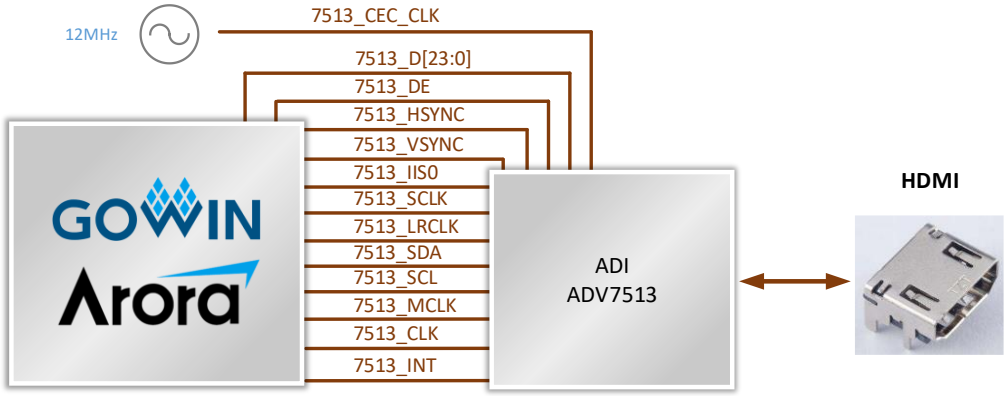
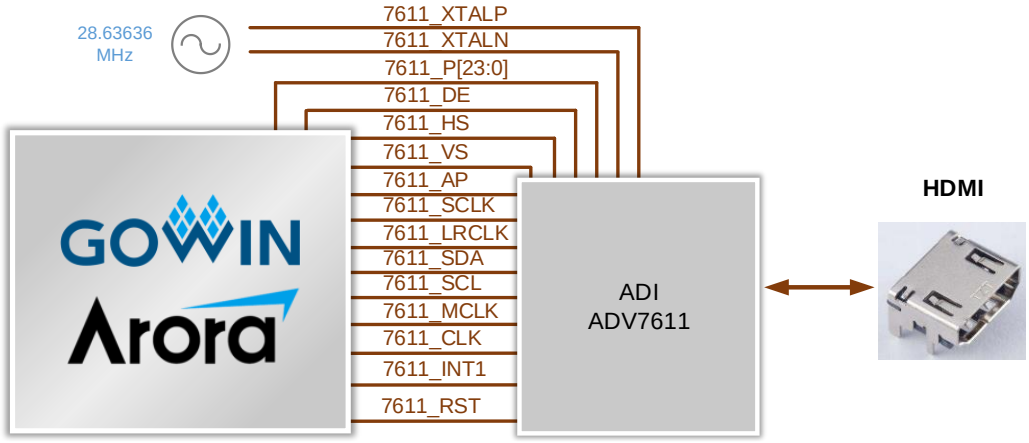


Figure 3-8 Connection Diagram of HDMI_RX Interface



3.8.2 Pin Distribution

Table 3-8 Pin Distribution of HDMI_TX Interface

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
7513_CLK	K18	5	3.3V	The RGB data row locks the output clock
7513_D0	P20	7	3.3V	RGB data signal
7513_D1	P19	7	3.3V	RGB data signal
7513_D2	P17	6	3.3V	RGB data signal
7513_D3	P16	6	3.3V	RGB data signal
7513_D4	P15	6	3.3V	RGB data signal
7513_D5	N20	5	3.3V	RGB data signal
7513_D6	N19	5	3.3V	RGB data signal
7513_D7	N17	6	3.3V	RGB data signal
7513_D8	N15	6	3.3V	RGB data signal
7513_D9	N18	5	3.3V	RGB data signal
7513_D10	M20	5	3.3V	RGB data signal
7513_D11	M18	5	3.3V	RGB data signal
7513_D12	M17	5	3.3V	RGB data signal
7513_D13	M16	5	3.3V	RGB data signal
7513_D14	M15	5	3.3V	RGB data signal
7513_D15	K17	5	3.3V	RGB data signal
7513_D16	K16	4	3.3V	RGB data signal
7513_D17	J17	5	3.3V	RGB data signal
7513_D18	J16	5	3.3V	RGB data signal
7513_D19	J15	4	3.3V	RGB data signal
7513_D20	H18	4	3.3V	RGB data signal
7513_D21	H17	4	3.3V	RGB data signal
7513_D22	H15	4	3.3V	RGB data signal
7513_D23	G18	4	3.3V	RGB data signal
7513_VS	R18	6	3.3V	Vertical synchronization signal

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
7513_HSYNC	R17	6	3.3V	Horizontal synchronization signal
7513_DE	R16	6	3.3V	RGB data enable
7513_SCLK	T16	2	3.3V	IIS interface SCLK
7513_LRCLK	T18	6	3.3V	IIS interface LRCLK
7513_MCLK	R19	7	3.3V	IIS interface MCLK
7513_IIS0	T15	6	3.3V	IIS interface data signal
7513_SCL	G16	4	3.3V	I2C serial interface clock
7513_SDA	G17	4	3.3V	I2C serial interface data
7513_INT	G15	4	3.3V	Interrupt signal

Table 3-9 Pin Distribution of HDMI_RX Interface

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
7611_CLK	U20	8	3.3V	The RGB data row locks the output clock
7611_P0	AA19	8	3.3V	RGB data signal
7611_P1	Y19	8	3.3V	RGB data signal
7611_P2	AB20	8	3.3V	RGB data signal
7611_P3	AA20	7	3.3V	RGB data signal
7611_P4	W19	8	3.3V	RGB data signal
7611_P5	AB21	8	3.3V	RGB data signal
7611_P6	AA21	7	3.3V	RGB data signal
7611_P7	Y21	8	3.3V	RGB data signal
7611_P8	AB22	8	3.3V	RGB data signal
7611_P9	W20	8	3.3V	RGB data signal
7611_P10	W21	7	3.3V	RGB data signal
7611_P11	Y22	8	3.3V	RGB data signal
7611_P12	V19	8	3.3V	RGB data signal
7611_P13	W22	8	3.3V	RGB data signal
7611_P14	V20	8	3.3V	RGB data signal
7611_P15	V18	8	3.3V	RGB data signal

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
7611_P16	U17	8	3.3V	RGB data signal
7611_P17	V22	7	3.3V	RGB data signal
7611_P18	U18	8	3.3V	RGB data signal
7611_P19	U16	6	3.3V	RGB data signal
7611_P20	U21	7	3.3V	RGB data signal
7611_P21	U15	6	3.3V	RGB data signal
7611_P22	T21	7	3.3V	RGB data signal
7611_P23	T20	7	3.3V	RGB data signal
7611_VS	AA18	8	3.3V	Vertical synchronization signal
7611_HS	AB18	8	3.3V	Horizontal synchronization signal
7611_DE	Y18	8	3.3V	RGB data enable
7611_SCLK	AB17	7	3.3V	IIS interface SCLK
7611_LRCLK	Y17	7	3.3V	IIS interface LRCLK
7611_MCLK	W17	8	3.3V	IIS interface MCLK
7611_AP	V17	8	3.3V	Audio input pin
7611_SCL	AB16	7	3.3V	I2C serial interface clock
7611_SDA	AA16	7	3.3V	I2C serial interface data
7611_INT1	Y16	7	3.3V	Interrupt signal
7611_RST	AB15	8	3.3V	System Reset

3.9 SDI Interface

3.9.1 Introduction

The development board includes SDI interfaces with 2-channel receivers and 2-channel transmitters. The 2-channel SDI-IN interface receives serial data via the BNC female; the SDI-OUT interface sends the processed serial data via the BNC female. The design diagram is shown in Figure 3-9.

Figure 3-9 Connection Diagram of SDI Interface

3.9.2 Pin Distribution

Table 3-10 Pin Distribution of SDI Interface

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
SDI_1_IN_P	B10	Q0	-	SDI+ input
SDI_1_IN_N	A10	Q0	-	SDI- input
SDI_2_IN_P	B8	Q0	-	SDI+ input
SDI_2_IN_N	A8	Q0	-	SDI- input
SDI_1_OUT_P	B6	Q0	-	SDI+ output
SDI_1_OUT_N	A6	Q0	-	SDI- output
SDI_2_OUT_P	B4	Q0	-	SDI+ output
SDI_2_OUT_N	A4	Q0	-	SDI- output

3.10 Ethernet Interface

3.10.1 Introduction

The development board leads 2-channel Ethernet interfaces, supporting RGMII (10BASE-T/100BASE-T/1000BASE-T) interfaces. Use the RJ45 connector integrated with network transformer internally. The connection diagram is shown in Figure 3-10.

Figure 3-10 Ethernet Interface Connection Diagram

3.10.2 Pin Distribution

Table 3-11 Ethernet Interface 1 Pin Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
PHY1_RXC	E19	2	3.3V	RGMII receive clock
PHY1_GTXCLK	H19	5	3.3V	RGMII transmit clock
PHY1_RXD3	C20	2	3.3V	RGMII/MII receive data
PHY1_RXDV	A19	2	3.3V	RGMII receive data, valid
PHY1_RXD2	D19	2	3.3V	RGMII/MII receive data
PHY1_RXD1	D20	2	3.3V	RGMII/MII receive data
PHY1_RXD0	D21	2	3.3V	RGMII/MII receive data
PHY1_TXEN	E21	2	3.3V	RGMII transmit enable
PHY1_TXD3	F19	2	3.3V	RGMII transmit data
PHY1_TXD2	F20	2	3.3V	RGMII transmit data
PHY1_TXD1	F21	2	3.3V	RGMII transmit data
PHY1_TXD0	G20	5	3.3V	RGMII transmit data
PHY_MDC	K19	5	3.3V	Management data clock
PHY_MDIO	J19	5	3.3V	Management data I/O
PHY_RST_N	H20	5	3.3V	Reset

Table 3-12 Ethernet Interface 2 Pin Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
PHY2_RXC	B17	1	3.3V	RGMII receive clock
PHY2_GTXCLK	B20	2	3.3V	RGMII transmit clock
PHY2_RXD3	B13	1	3.3V	RGMII/MII receive data
PHY2_RXDV	C13	1	3.3V	RGMII receive data, valid
PHY2_RXD2	A13	1	3.3V	RGMII/MII receive data
PHY2_RXD1	C14	1	3.3V	RGMII/MII receive data
PHY2_RXD0	A14	1	3.3V	RGMII/MII receive data
PHY2_TXEN	A15	1	3.3V	RGMII transmit enable

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
PHY2_TXD3	A16	1	3.3V	RGMII transmit data
PHY2_TXD2	B16	1	3.3V	RGMII transmit data
PHY2_TXD1	B15	1	3.3V	RGMII transmit data
PHY2_TXD0	A20	2	3.3V	RGMII transmit data
PHY_MDC	K19	5	3.3V	Management data clock
PHY_MDIO	J19	5	3.3V	Management data I/O
PHY_RST_N	H20	5	3.3V	Reset

3.11 MIPI Interface

3.11.1 Introduction

The development board leads one dual-channel MIPI interface from the FPGA, each with 4 Data and 1 Clk. The MIPI interface connects to the MIPI D-PHY RX/TX soft core in the FPGA and also provides four GPIOs with 3.3V logic levels, power supply, and ground. This interface uses an 80P AXK580147YG connector with 0.5mm pitch. The connection diagram of MIPI interface is shown in Figure 3-11.

Figure 3-11 Connection Diagram of MIPI Interface

3.11.2 Pin Distribution

Table 3-13 Pin Distribution of MIPI Interface

J12 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	M0_D0N	J6	10	1.8V	MIPI data signal
2	NC	-	-	-	Floating
3	M0_D0P	K6	10	1. 8V	MIPI data signal
4	NC	-	-	-	Floating
5	GND	-	-	-	GND
6	GND	-	-	-	GND
7	M0_D1N	J4	10	1.8V	MIPI data signal
8	GND	-	-	-	GND
9	M0_D1P	K4	10	1.8V	MIPI data signal
10	GND	-	-	-	GND
11	GND	-	-	-	GND
12	NC	-	-	-	Floating
13	M0_CKN	K3	10	1.8V	MIPI clock signal
14	NC	-	-	-	Floating
15	M0_CKP	L3	10	1.8V	MIPI clock signal
16	GND	-	-	-	GND
17	GND	-	-	-	GND
18	GND	-	-	-	GND
19	M0_D2N	L4	10	1.8V	MIPI data signal
20	GND	-	-	-	GND
21	M0_D2P	L5	10	1.8V	MIPI data signal
22	NC	-	-	-	Floating
23	GND	-	-	-	GND
24	NC	-	-	-	Floating
25	M0_D3N	L1	10	1.8V	MIPI data signal
26	NC	-	-	-	Floating

J12 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
27	M0_D3P	M1	10	1.8V	MIPI data signal
28	GND	-	-	-	GND
29	GND	-	-	-	GND
30	GND	-	-	-	GND
31	M1_D0N	M5	10	1.8V	MIPI data signal
32	NC	-	-	-	Floating
33	M1_D0P	M6	10	1.8V	MIPI data signal
34	NC	-	-	-	Floating
35	GND	-	-	-	GND
36	GND	-	-	-	GND
37	M1_D1N	M2	10	1.8V	MIPI data signal
38	GND	-	-	-	GND
39	M1_D1P	M3	10	1.8V	MIPI data signal
40	GND	-	-	-	GND
41	GND	-	-	-	GND
42	NC	-	-	-	Floating
43	M1_CKN	N5	10	1.8V	MIPI clock signal
44	NC	-	-	-	Floating
45	M1_CKP	P6	10	1.8V	MIPI clock signal
46	GND	-	-	-	GND
47	GND	-	-	-	GND
48	GND	-	-	-	GND
49	M1_D2N	N3	10	1.8V	MIPI data signal
50	GND	-	-	-	GND
51	M1_D2P	N4	10	1.8V	MIPI data signal
52	MIPI_GPIO1	J2	11	3.3V	GPIO
53	GND	-	-	-	GND
54	MIPI_GPIO2	K2	11	3.3V	GPIO
55	M1_D3N	P4	10	1.8V	MIPI data signal

J12 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
56	MIPI_GPIO3	J1	11	3.3V	GPIO
57	M1_D3P	P5	10	1.8V	MIPI data signal
58	MIPI_GPIO4	K1	11	3.3V	GPIO
59	GND	-	-	-	GND
60	GND	-	-	-	GND
61	NC	-	-	-	Floating
62	NC	-	-	-	Floating
63	NC	-	-	-	Floating
64	NC	-	-	-	Floating
65	GND	-	-	-	GND
66	GND	-	-	-	GND
67	NC	-	-	-	Floating
68	NC	-	-	-	Floating
69	NC	-	-	-	Floating
70	NC	-	-	-	Floating
71	GND	-	-	-	GND
72	GND	-	-	-	GND
73	NC	-	-	-	Floating
74	GND	-	-	-	GND
75	NC	-	-	-	Floating
76	VCC3P3	-	-	3.3V	Power
77	GND	-	-	-	GND
78	VCC3P3	-	-	3.3V	Power
79	GND	-	-	-	GND
80	VCC3P3	-	-	3.3V	Power

3.12 LVDS Interface

3.12.1 Introduction

The board leads out two LVDS interfaces connecting 10 pairs of differential signals, including 8 Data and 2 Clk; the interface uses two 2x10P headers with 2.0mm pitch. The connection diagram is shown in Figure 3-12.

Figure 3-12 Connection Diagram of LVDS Interface

3.12.2 Pin Distribution

Table 3-14 Pin Distribution of LVDS Interface

J13 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	LVDS25_P1	B21	2	3.3V	LVDS data
2	LVDS25_N1	A21	2	3.3V	LVDS data
3	GND	-	-	-	GND
4	GND	-	-	-	GND
5	LVDS25_P2	C22	2	3.3V	LVDS data
6	LVDS25_N2	B22	2	3.3V	LVDS data
7	GND	-	-	-	GND
8	GND	-	-	-	GND
9	LVDS25_CK_P1	C18	2	3.3V	LVDS clock
10	LVDS25_CK_N1	C19	2	3.3V	LVDS clock
11	GND	-	-	-	GND
12	GND	-	-	-	GND

J13 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
13	LVDS25_P3	E22	2	3.3V	LVDS data
14	LVDS25_N3	D22	2	3.3V	LVDS data
15	GND	-	-	-	GND
16	GND	-	-	-	GND
17	LVDS25_P4	G21	2	3.3V	LVDS data
18	LVDS25_N4	G22	2	3.3V	LVDS data
19	GND	-	-	-	GND
20	GND	-	-	-	GND

J14 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	LVDS25_P5	J22	5	3.3V	LVDS data
2	LVDS25_N5	H22	5	3.3V	LVDS data
3	GND	-	-	-	GND
4	GND	-	-	-	GND
5	LVDS25_P6	K21	5	3.3V	LVDS data
6	LVDS25_N6	K22	5	3.3V	LVDS data
7	GND	-	-	-	GND
8	GND	-	-	-	GND
9	LVDS25_CK_P2	J20	5	3.3V	LVDS clock
10	LVDS25_CK_N2	J21	5	3.3V	LVDS clock
11	GND	-	-	-	GND
12	GND	-	-	-	GND
13	LVDS25_P7	M21	5	3.3V	LVDS data
14	LVDS25_N7	L21	5	3.3V	LVDS data
15	GND	-	-	-	GND
16	GND	-	-	-	GND
17	LVDS25_P8	N22	5	3.3V	LVDS data

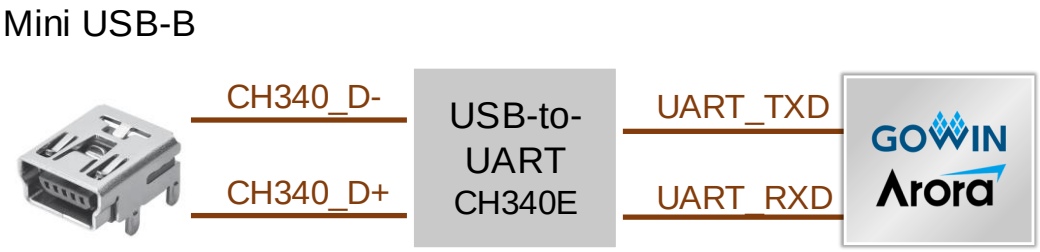
J14 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
18	LVDS25_N8	M22	5	3.3V	LVDS data
19	GND	-	-	-	GND
20	GND	-	-	-	GND

3.13 UART Interface

3.13.1 Introduction

The UART interface led from the development board uses Mini USB-B connector, which is implemented via USB conversion chips. The connection diagram of UART interface is shown in Figure 3-13.

Figure 3-13 Connection Diagram of UART Interface



3.13.2 Pin Distribution

Table 3-15 Pin Distribution of UART Interface

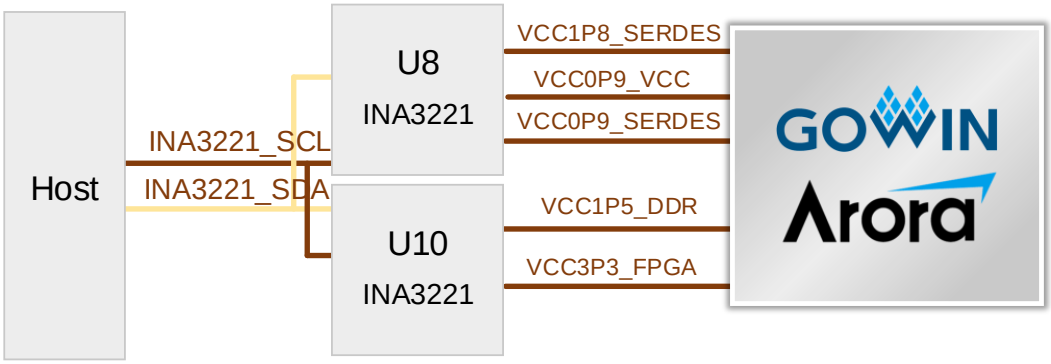
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
UART_TXD	H2	11	3.3V	The serial port data input to FPGA
UART_RXD	H3	11	3.3V	The serial port data output by FPGA

3.14 I2C Interface

3.14.1 Introduction

The development board includes 1-channel I2C interface as the host communication interface. The host can monitor the power consumption of FPGA VCC, VCCX, SerDes, and each BANK through this interface. The connection diagram of I2C interface is shown in Figure 3-14.

Figure 3-14 Connection Diagram of I2C Interface



3.14.2 Pin Distribution

Table 3-16 Pin Distribution of I2C Interface

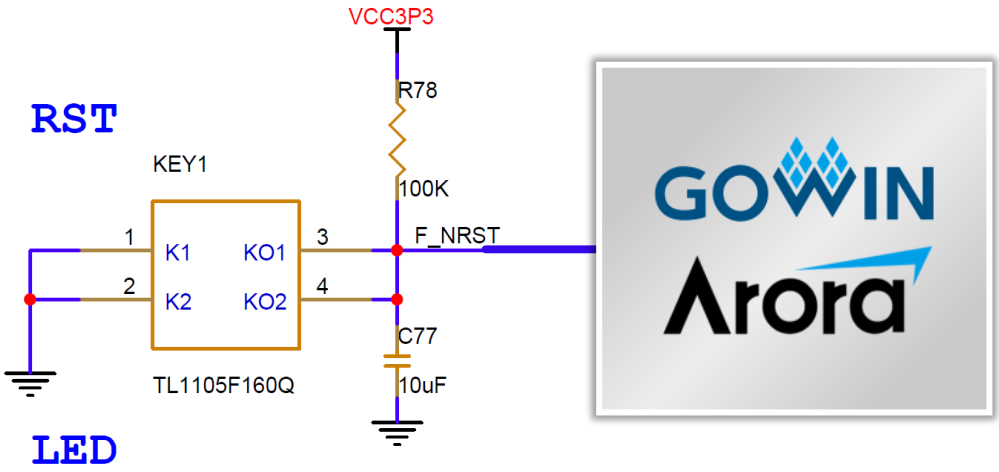
J17 Pin No.	Signal Name	I/O Level	Description
1	GND	-	GND
2	INA3221_SCL	3.3V	Serial bus clock line
3	GND	-	GND
4	INA3221_SDA	3.3V	Serial bus data line

3.15 Key & LED

3.15.1 Introduction

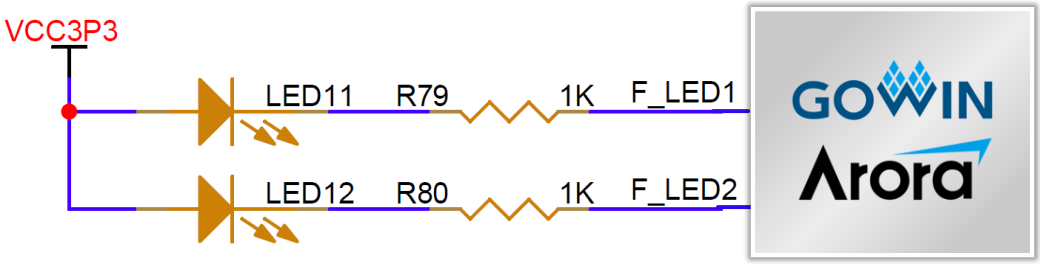
The development board includes one reset key, which is connected to the general IO of FPGA BANK11. The corresponding IO input voltage of the FPGA is low when the key is pressed while high when the key is not pressed. The connection diagram is shown in Figure 3-15.

Figure 3-15 Connection Diagram of Key



The development board includes two user LEDs. The user LED is connected to the IO of FPGA BANK11 and can be switched on and off via the program. When the IO voltage is high, it will be on; When the IO voltage is low, it will be off. The connection diagram is shown in Figure 3-16.

Figure 3-16 Connection Diagram of LED



3.15.2 Pin Distribution

Table 3-17 Pin Distribution of Key

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_NRST	H4	11	3.3V	Reset Key

Table 3-18 Pin Distribution of Indicator

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_LED1	J5	11	3.3V	LED indicator
F_LED2	H5	11	3.3V	LED indicator

3.16 GPIO

3.16.1 Introduction

The development board leads ten GPIOs with 3.3V voltage level standard through one 2*7P pin header with 2.54 mm pitch, facilitating user testing. The GPIO interfaces are designed with ESD protection circuit.

Figure 3-17 Connection Diagram of GPIO Interface

3.16.2 Pin Distribution

Table 3-19 Pin Distribution of GPIO Interface

J2 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	F_GPIO0	E17	1	3.3V	GPIO
2	F_GPIO1	F16	1	3.3V	GPIO
3	F_GPIO2	E16	1	3.3V	GPIO
4	F_GPIO3	F15	1	3.3V	GPIO
5	F_GPIO4	C15	1	3.3V	GPIO
6	F_GPIO5	D15	1	3.3V	GPIO

J2 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
7	F_GPIO6	D14	1	3.3V	GPIO
8	F_GPIO7	E14	1	3.3V	GPIO
9	F_GPIO8	F14	1	3.3V	GPIO
10	F_GPIO9	E13	1	3.3V	GPIO
11	VCC3P3	-	-	3.3V	Power
12	VCC3P3	-	-	3.3V	Power
13	GND	-	-	-	GND
14	GND	-	-	-	GND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